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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 08/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,483	HOOKER, RODNEY E.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5 and 9-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5 and 9-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *see attached*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS: 12/12/05, 1/23/06*.

8/10/06
6/30/06
6/21/06
6/05/06
5/24/06

DETAILED ACTION

Specification

1. The changes made to the specification made on 6/13/06 are approved.

Claim Rejections - 35 USC § 112

2. The amendments made to claim 19 made on 6/13/06 overcome the rejection made under 35 USC 112.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 3-5, 9-12, 16-18, 20, 23-25, and 32-39 are rejected under 35 U.S.C. 102(b) as being anticipated by Lynch, US Patent 5,930,820.

5. With respect to claim 1, Lynch teaches a variable latency cache memory, comprising:

an input, for specifying a type of an instruction requesting to read data from the cache memory, wherein said type is one of a plurality of predetermined instruction types, in col. 6, lines 56-60;

a plurality of storage elements, coupled to said input, configured as a last-in-first-out (LIFO) memory, for providing said data in a first number of clock cycles if said input specifies a pop instruction type of said plurality of predetermined instruction types, and for providing said data in a second number of clock cycles if said input specifies a load instruction type of said plurality of predetermined instruction types, wherein said first and second number of clock cycles is different, in col. 6, lines 26-39. The first predetermined type of Lynch corresponds to the case in which data is stored in the top of the cache. The second predetermined type of instruction occurs when the data is not in the top of the cache, which takes more clock cycles. Referring to fig. 2, Data Cache 34 is the first plurality of storage elements.

6. With respect to claim 3, Lynch teaches the cache memory of claim 1, further comprising:

a second plurality of storage elements, coupled to said first plurality of storage elements, for caching non-stack data, whereas said first plurality of storage elements is for caching stack data, in fig. 1, main memory 16.

7. With respect to claim 4, Lynch teaches the cache memory of claim 3, wherein said second plurality of storage elements provides said data in a third number of clock cycles if said data is not present in said first plurality of storage elements and if said input specifies said load instruction type of said plurality of predetermined instruction types, where said second and third number of clock cycles is different, in col. 1, lines 31-40.

8. With respect to claim 5, Lynch teaches the cache memory of claim 4, wherein said third number of clock cycles is greater than said second number of clock cycles, in col. 1, lines 31-40.

9. With respect to claim 9, Lynch teaches the cache memory of claim 1, a computer program product comprising a computer usable medium having computer readable program code causes the cache memory, wherein said computer program product is for use with a computing device, in col. 4, lines 17-22.

10. With respect to claim 10, Lynch teaches a variable latency cache memory, comprising:

a plurality of storage elements, configured as a last-in-first-out (LIFO) memory, having first and second subsets of said plurality of storage elements, said first subset for caching stack data more recently pushed than data cached in said second subset, in col. 3, lines 18- 25.

an input, for specifying a memory address of source data requested from the cache memory, in fig. 3, Address 64.

at least one comparator, coupled to said input, for comparing said memory address with one or more memory addresses of said data cached in said first subset of storage elements, wherein if said memory address hits in said first subset based on said comparing, the cache memory provides said source data from said first subset in a first number of clock cycles, wherein if said memory address does not hit in said first subset but hits in said second subset based on said comparing, the cache memory provides

said source data from said second subset in a second number of clock cycles, wherein said first and second number of cycles is different, in col. 6, lines 23-39.

11. With respect to claim 11, Lynch teaches the cache memory of claim 10, wherein said first number of clock cycles is less than said second number of clock cycles, in col. 6, lines 23-39.

12. With respect to claim 12, Lynch teaches the cache memory of claim 10, wherein said address comprises a virtual address, in col. 1, line 62 through col. 2, line 12. A tag address is a virtual representation of the actual physical address.

13. With respect to claim 16, Lynch teaches the cache memory of claim 10, further comprising:

a second plurality of storage elements coupled to said first plurality of storage elements, for caching non-stack data, in fig. 1, main memory 16.

14. With respect to claim 17, Lynch teaches the cache memory of claim 16, wherein said second plurality of storage of storage elements provides said data in a third number of clock cycles if said address does not hit in said first plurality of storage elements, wherein said second and third number of clock cycles is different, in col. 1, lines 31-40.

15. With respect to claim 18, Lynch teaches the cache memory of claim 17, wherein said third number of clock cycles is greater than said second number of clock cycles, in col. 1, lines 31-40.

16. With respect to claim 20, Lynch teaches the cache memory of claim 10, wherein said first subset comprises a top one of said plurality of storage elements, in col. 9, lines 52-56. When a standard pop command is performed, the top one of the storage elements is accessed.

17. With respect to claim 23, Lynch teaches the cache memory of claim 10, wherein said memory address comprises a source data address of a load instruction, in col. 1, line 62 through col. 2, line 4.

18. With respect to claim 24, Lynch teaches the cache memory of claim 19, wherein a computer data signal embodied in a transmission medium comprising computer-readable program code provides the cache memory, in col. 4, lines 17-22.

19. With respect to claim 25, Lynch teaches the cache memory of claim 10, wherein a computer program product comprising a computer usable medium having computer readable program code causes the cache memory, wherein said computer program product is for use with a computing device, in col. 4, lines 17-22.

20. With respect to claim 32, Lynch teaches a method for providing data from a last-in-first-out (LIFO) cache memory with a variable latency, the method comprising:

determining whether a request for data from the LIFO cache memory is in response to a pop or load instruction, in col. 6, lines 26-34;

providing the data from the LIFO cache memory in a first number of clock cycles if the request is in response to a pop instruction, in col. 4, lines 46-52, as well as in col. 6, lines 36-39 and col. 11, lines 34-39;

providing the data from the LIFO cache memory in a second number of clock cycles if the request is in response to a load instruction, wherein the first and second number of clock cycles is different, in col. 46, lines 46-48. It is disclosed in the sections of the reference listed above that this conventional load instruction takes more clock cycles than the stack pop instruction.

21. With respect to claim 33, Lynch teaches the method of claim 32, wherein the first number of clock cycles is less than the second number of clock cycles, in col. 4, lines 46-52.

22. With respect to claim 34, Lynch teaches the method of claim 32, wherein said providing the data in the first number of clock cycles if the request is in response to a pop instruction is speculative subject to a subsequent determination that a source address of the data hits in the cache memory, in col. 2, lines 56-61.

23. With respect to claim 35, Lynch teaches the method of claim 32, wherein a load instruction comprises an instruction explicitly specifying a source address of the data, in col. 1, line 62 through col. 2, line 12.

24. With respect to claim 36, Lynch teaches the method of claim 32, wherein a pop instruction comprises an instruction inherently specifying a source address of the data, in col. 4, lines 46-47.

25. With respect to claim 37, Lynch teaches the method of claim 36, wherein the pop instruction inherently specifies the source address of the data relative to a stack pointer value, in col. 6, lines 6-13.

26. With respect to claim 38, Applicant claims a computer program product embodied in a computer-readable medium, comprising computer-readable program code for providing the variable latency cache memory of claim 1, and is therefore rejected using similar logic.

27. With respect to claim 39, Applicant claims a computer program product embodied in a computer-readable medium for providing the variable latency cache memory of claim 10, and is therefore rejected using similar logic.

28. Claim 26 is rejected under 35 U.S.C. 102(b) as being anticipated by Mathews, US Patent 5,956,752.

29. Mathews teaches storing stack data into the cache memory in a last-in-first-out manner, in col. 5, lines 20-27.

providing load data from the cache memory in a first number of clock cycles if a virtual memory address of the load data hits in the cache memory, in col. 5, lines 28-36 ; and

providing the load data from the cache memory in a second number of clock cycles if the virtual memory address of the load data misses in the cache memory but a physical memory address of the load data hits in the cache memory, wherein the first and second number of clock cycles is different, in col. 5, lines 28-36. When the predicted (virtual) address does not hit, another step is taken and the physical address is used, thereby using more clock cycles.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

32. Claims 13-15 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch as applied to claims 1, 3-5, 9-12, 16-18, 20, 23-25, and 32-39 above, in view of Mathews. Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathews as applied to claim 26 above, in view of Lynch.

33. With respect to claim 13, Lynch teaches all other limitations of the parent claims but fails to expressly teach a physical memory address. Mathews teaches a second input, coupled to said plurality of storage elements, for specifying a physical memory address of said source data requested from the cache memory, in fig. 5, Physical Address 122.

34. It would have been obvious to one of ordinary skill in the art having the teachings of Lynch and Mathews before him at the time the invention was made, to combine the

memory access system of Lynch with the memory access system of Mathews because by using an initial access of the cache using a virtual address, you eliminate the access latency required to translate to a physical address, as taught by Mathews in col. 2, lines 29-31. In addition, a virtual addressing scheme allows the use of memory management mechanisms such as segmentation and paging, as taught by Mathews in col. 1, lines 20-28.

35. With respect to claim 14, Mathews teaches the cache memory of claim 13, further comprising:

a second at least one comparator, coupled to receive said second input, for comparing said physical memory address with one or more physical memory addresses of said data cached in said first subset of storage elements, in fig. 5, comparator 140.

36. With respect to claim 15, Mathews teaches the cache memory of claim 14, further comprising:

an output, coupled to said first and second at least one comparator, for indicating an error condition if the cache memory provides said source data from said first subset based on said comparing said virtual memory address with said one or more memory address of said data cached in said first subset of storage elements, but said second at least one comparator indicates said physical memory address does not match any of said one or more physical memory addresses of said data cached in said first subset of storage elements, in fig. 5, prediction wrong output 178.

37. With respect to claim 19, Lynch teaches all other limitations of the parent claim but fails to teach a physical address compare. Mathews teaches the cache memory of

claim 10, wherein if said address does not hit in said first subset based on said comparing, the cache memory provides said source data in said second number of clock cycles based on a physical compare, in col. 5, lines 28-36. When the predicted (virtual) address does not hit, another step is taken and the physical address is used, thereby using more clock cycles.

38. It would have been obvious to one of ordinary skill in the art having the teachings of Lynch and Mathews before him at the time the invention was made, to combine the memory access system of Lynch with the memory access system of Mathews because by using an initial access of the cache using a virtual address, you eliminate the access latency required to translate to a physical address, as taught by Mathews in col. 2, lines 29-31. In addition, a virtual addressing scheme allows the use of memory management mechanisms such as segmentation and paging, as taught by Mathews in col. 1, lines 20-28.

39. With respect to claim 27, Mathews teaches all other limitations of the parent claim as discussed supra. Mathews also teaches the use of a virtual memory address, but fails to teach the limitations of claim 27. Lynch teaches the method of claim 26, further comprising:

determining whether the memory address hits in a top subset of cache lines of the cache memory, wherein the top subset is less than all cache lines of the cache memory, in col. 6, lines 26-28.

40. It would have been obvious to one of ordinary skill in the art having the teachings of Lynch and Mathews before him at the time the invention was made, to combine the

memory access system of Lynch with the memory access system of Mathews because by using an initial access of the cache using a virtual address, you eliminate the access latency required to translate to a physical address, as taught by Mathews in col. 2, lines 29-31. In addition, a virtual addressing scheme allows the use of memory management mechanisms such as segmentation and paging, as taught by Mathews in col. 1, lines 20-28.

41. With respect to claim 28, Lynch teaches the method of claim 27, wherein the top subset of cache lines of the cache memory comprises cache lines implicated by the most recently pushed stack data, in col. 6, lines 26-28 and col. 2, lines 22-24.

42. With respect to claim 29, Lynch teaches the method of claim 26, wherein the first number of clock cycles is less than the second number of clock cycles, in col. 4, lines 46-52.

43. With respect to claim 30, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that loaded data is speculative subject to determination of a physical address. Mathews teaches providing the load data from the cache memory in the first number of clock cycles if the virtual memory address of the load data hits in the cache memory is speculative subject to a subsequent determination that the physical memory address of the load data hits in the cache memory, in col. 5, lines 28-36.

44. With respect to claim 31, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that loaded data is speculative subject to determination of a physical address. Mathews teaches providing the load data from a

non-stack cache memory in a third number of clock cycles if the virtual memory address and the physical memory address miss in the cache memory, wherein the first and third number of clock cycles is different, in col. 5, lines 28-36.

45. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch as applied to claims 1, 3-5, 9-12, 16-18, 20, 23-25, and 32-39 above, in view of Healey, US Patent 3,810,117.

46. With respect to claim 21, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that the offset in the cache memory which controls the size of the first plurality of storage elements can be precisely two. Healey teaches separating the first X number of entries from the top of the stack in order to have faster access to them, in col. 1, lines 24-39. It is disclosed that the top two entries in the stack can form a subset in col. 1, lines 46-54, thereby teaching:

The cache memory of claim 10, said first subset comprises a top two of said plurality of storage elements.

47. It would be obvious to one of ordinary skill in the art at the time the invention was made to modify the stack cache storage system of Lynch with the stack cache storage system of Healey in order to have a small subset of stack elements that are quicker and easier to access than the rest of the storage, as taught by Healey in col. 1, lines 17-23.

48. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lynch as applied to claims 1-3, 7-12, 16, 20, 23-29, and 32-39 above, in view of Tremblay et al., US Patent 6,038,643.

49. With respect to claim 22, Lynch teaches all other limitations of the parent claims as discussed supra but fails to expressly teach that the offset in the cache memory which controls the size of the first plurality of storage elements can be precisely three. The Healey reference used above for claim 22 teaches separating the first X number of entries from the top of the stack in order to have faster access to them. The Healey reference also fails to expressly disclose that the number of items can be three. Tremblay et al. resolves this deficiency in the prior art by keeping the top three elements of the stack in a separate, faster storage area in col. 18, lines 51-58, thereby teaching the limitation:

The cache memory of claim 10, wherein said first subset comprises a top three of said plurality of storage elements.

50. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the stack cache storage system of Lynch with the stack cache storage system of Healey in order to have a small subset of stack elements that are quicker and easier to access than the rest of the storage, as taught both by Healey in col. 1, lines 17-23, as well as by Tremblay et al., in col. 18, lines 51-55.

Response to Arguments

51. In response to Applicant's arguments on pages 9-14, filed 6/14/06 in regards to the rejections under 35 U.S.C. 102(b) and 35 U.S.C. 103(a), the examiner has modified the prior art rejection to more clearly show how the prior art teaches the pending claims 1, 3-5, and 9-39.

52. The examiner did not reject claims 13-15 due to an oversight in the first Office Action. Claims 13-15 are rejected in this Office Action, and subsequently this action is non-final.

53. With respect to claim 1, the Examiner has clarified the rejection to show that the Lynch reference teaches the limitations. In the present rejection, the Data Cache 34 of fig. 2 is taken as a whole to read on the first plurality of storage elements. This data cache 34 is organized as a LIFO memory because a portion of the memory acts as stack storage. Accordingly, the stack and non-stack portions are part of the same plurality of memory. This appears to the same way Applicant implements the LIFO (fig. 1 data cache 126). The second plurality of storage elements is the Main Memory 16 in fig. 1. The first number of clock cycles is when the data hits in the stack pop operation. The second number of clock cycles is when the load/store unit supplies a load instruction and the accompanying data address to the data cache 34 in response to a miss in the stack portion. The third number of clock cycles occurs when it misses data cache 34 altogether, and an access to main memory is performed.

54. With respect to claim 10, the Examiner clarified the above rejection, similar to claim 1.

55. With respect to claim 20, the claim remains rejected because the comparison is not between a pop operation and a stack access operation but between a pop operation and either a load from the data cache or access to main memory.

56. With respect to claim 26, the Examiner withdrew the rejection under Lynch and rejected it instead with Mathews, due to the fact that Lynch is silent on virtual memory addressing.

57. With respect to claim 32, the Examiner clarified the above rejection, similar to claim 1.

Conclusion

58. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar cache memory storage systems.

59. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
August 21, 2006

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